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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,257	01/02/2004	Kwon O. Sung	10808/121	7472

48581 7590 11/15/2005

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EXAMINER	
CHEN, ERIC BRICE	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/751,257	SUNG, KWON O.	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *16-20* is/are withdrawn from consideration.

5)☒ Claim(s) *1-10* is/are allowed.

6)☒ Claim(s) *11-15* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Invention I, claims 1-15, in the reply filed on Sept. 26, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Priority

2. Applicant is advised of possible benefits under 35 U.S.C. 119(a)-(d), wherein an application for patent filed in the United States may be entitled to the benefit of the filing date of a prior application filed in a foreign country.

Claim Objections

3. Claim 11 objected to because of the following informalities: the claim language "providing an undoped polysilicon layer over said *undoped* portion of said polysilicon layer" (emphasis added) apparently should be -- providing an undoped polysilicon layer over said *doped* portion of said polysilicon layer -- (emphasis added). Otherwise, the claim language would be inconsistent with the Specification (page 16, lines 4-7) and Figure 2C. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 11 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Cheek et al. (U.S. Patent No. 6,261,885).

6. As to claim 11, Cheek discloses a method of manufacturing a layer sequence having a first (106A) and a second laterally confined structure (106B) (Figure 9), comprising the steps of: providing a gate oxide layer (104) on a substrate (100) (column 7, lines 16-19; Figure 2); providing a polysilicon layer having an undoped portion (110) (column 7, lines 41-43) (region 106A in Figures 3-4) to form a gate of a p-MOS transistor (122A) (column 8, lines 44-47; Figure 8) and a doped portion (column 7, lines 41-43; region 106B in Figure 4) to form a gate of an n-MOS transistor (122B) (column 8, lines 47-51; Figure 8); providing a doped polysilicon layer (116) over said undoped portion of said polysilicon layer (110) (region 106A in Figure 6); and providing an undoped polysilicon layer over said (116) doped portion of said polysilicon layer (110) (column 8, lines 4-6) (region 106B in Figure 6).

7. As to claim 15, Cheek discloses a step of etching said gate of said p-MOS transistor and said gate of said n-MOS transistor to have approximately equal dimensions (column 8, lines 51-53; Figures 7-8).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheek in view of Gardner et al. (U.S. Patent No. 5,854,115).

11. As to claim 12, Cheek does not expressly disclose a step of providing a hard mask layer over said polysilicon layer. However, Gardner discloses a method of forming a transistor gate structure (column 1, lines 8-13), including forming etch stop (58) below the surface of polysilicon layer (56) (column 5, lines 5-11; Figure 3A). Etch stop (58) functions as a hard mask because it prevents etching of polysilicon region (56B) (column 5, lines 55-63; Figures 5-6). Moreover, Gardner teaches that incorporating an etch stop in the polysilicon layer provides for better control of the profile

during etching (column 3, lines 2-17). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a hard mask layer over said polysilicon layer. One who is skilled in the art would be motivated to adopt a method which provides for improved control over the etching profile.

Claim Rejections - 35 USC § 103

12. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheek in view of Wolf, *Silicon Processing for the VLSI Era*, Vol. 4, Lattice Press (2002).

13. As to claim 13, Cheek does not expressly disclose providing a bottom antireflective coating over said doped polysilicon layer and said undoped polysilicon layer. However, Cheek discloses pattering doped polysilicon layer (110/116, regions 106A/106B) and said undoped polysilicon layer (110/116, regions 106A/106B) (column 8, lines 39-44; Figure 8), including the application of a layer of photoresist (column 3, lines 60-63). Wolf teaches that anti-reflective coatings are often deposited between the substrate and photoresist to minimize standing waves and reflective notching from substrate reflections, and as a result, maintaining control over critical dimensions (pages 244-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to providing a bottom antireflective coating over said doped polysilicon layer and said undoped polysilicon layer. One who is skilled in the art would be motivated to form an anti-reflective coating to maintain control over critical dimensions.

Claim Rejections - 35 USC § 103

14. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheek in view of Callister, *Materials Science and Engineering*, 4th ed., John Wiley & Sons (1997).

15. As to claim 14, Cheek does not expressly disclose providing a doped polysilicon layer over said undoped portion of said polysilicon layer comprises doping said polysilicon layer over said undoped portion with approximately equal doping to said doped portion of said polysilicon layer. However, Callister teaches that conductivity of the silicon is directly proportionate (Equation (19.16), page 607; Equation (19.17), page 608) to the doping concentration of the semiconductor material (page 609). Moreover, because electrical conductivity varies with doping level, doping level appears to appears to reflect a result-effective variable which can be optimized. *See* MPEP § 2144.05 II. Doping level can be varied according, depending on the desired electrical properties. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a doped polysilicon layer over said undoped portion of said polysilicon layer comprises doping said polysilicon layer over said undoped portion with approximately equal doping to said doped portion of said polysilicon layer. One who is skilled in the art would be motivated to optimize through routine experimentation of dopant concentrations to achieve the desired electrical properties. *See* MPEP § 2144.05 II.

Allowable Subject Matter

16. Claims 1-10 are allowed.

17. The following is an examiner's statement of reasons for allowance: the prior art fails to teach or suggest forming a fourth layer on the second layer, which forth layer is doped *with dopant of the first type of conductivity* (emphasis added). The closest prior art, Cheek, discloses a method of manufacturing a layer sequence having a first (106A) and a second laterally confined structure (106B), comprising the steps of: providing a first layer (110) on a first surface portion of a substrate (100) (region 106B in Figure 3), which first layer is doped with dopant of a first type of conductivity (column 7, lines 34-36, 41-43; region 106B in Figure 4); providing a second layer (110) on a second surface portion of the substrate (region 106A in Figure 3), which second layer is free of dopant of the first type of conductivity (column 7, lines 41-43); forming a third layer (116) on the first layer (110) (region 106B in Figure 6), which third layer is free of dopant of the first type of conductivity (column 8, lines 4-13); forming a fourth layer (116) on the second layer (110) (region 106A in Figure 6), *which forth layer is doped with dopant of a second type of conductivity* (column 8, lines 4-13). However, there is no suggestion of motivation of forming a fourth layer on the second layer, which forth layer is doped with dopant of the first type of conductivity, as in the context of claim 1.

18. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Brown et al. (U.S. Patent No. 6,703,269) and Park (U.S. Patent No. 6,168,998) disclose a method of forming a semiconductor structure with a undoped polysilicon layer overlying a doped polysilicon layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC EBC
Oct. 28, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER